

**WHAT WE CLAIM IS:**

1. A processor, operable to execute instructions on a predicated basis, comprising:

5 a series of predicate registers, each switchable between at least respective first and second states and each assignable to one or more predicated-execution instructions;

10 a control information holding unit which holds items of control information corresponding respectively to said predicate registers of said series; and

15 a plurality of operating units, corresponding respectively to said predicate registers, each having a first control input connected to said control information holding unit for receiving the control-information item corresponding to the operating unit's own corresponding predicate register and also having a second control input connected for receiving the control-information item corresponding to a further one of said predicate registers, and operable to perform a state determining operation in which said state of its said own predicate register is determined in dependence upon the received control-information items, said operating units of the plurality being operable in parallel with one another to perform respective such state determining operations.

20 2. A processor as claimed in claim 1, wherein, for each said predicate register other than the last predicate register of said series, said further one of the predicate registers is the register following said own predicate register in said series.

25 3. A processor as claimed in claim 1, wherein each said operating unit also has at least one state input connected for receiving an item of state information, indicating said state of a predetermined one of said predicate registers of said series, and is operable to set the state of its said own predicate

register in dependence also upon said state-information item.

4. A processor as claimed in claim 3, wherein,  
for each said operating unit, said state-information  
5 item indicates said state of the unit's said own  
predicate register.

5. A processor as claimed in claim 3, wherein  
each said operating unit has respective first and  
second such state inputs connected for receiving  
10 respective such state-information items, indicating the  
respective states of two different ones of said  
predicate registers, and is operable to set the state  
of its said own predicate register in dependence also  
upon said state-information items.

15 6. A processor as claimed in claim 5, wherein,  
for each said operating unit, said two predicate  
registers are the unit's said own predicate register  
and the predicate register that precedes said own  
predicate register in said series.

20 7. A processor as claimed in any preceding  
claim, wherein the items of control information are  
changeable in use of the processor.

8. A processor as claimed in claim 1, wherein  
each said operating unit is operable selectively to  
25 perform any one of a plurality of different such state  
determining operations.

9. A processor as claimed in claim 8, wherein  
each said operating unit has a selection input for  
receiving one or more selection signals, and said state  
30 determining operation to be performed by the operating  
unit is selected by said one or more selection signals  
applied thereto.

10. A processor as claimed in claim 1, wherein  
each said control-information item is changeable  
35 between at least first and second values.

11. A processor as claimed in claim 10, wherein the or one said state determining operation is an initialisation operation in which each operating unit sets its said own predicate register to said second state in the event that the control-information item corresponding to that predicate register has said first value.

12. A processor as claimed in claim 11, wherein in said initialisation operation each said operating unit sets its said own predicate register to said first state in the event that the control-information item corresponding to that predicate register has said second value, and that said control-information item corresponding to the predicate register following said own predicate register in said series has said first value.

13. A processor as claimed in claim 10, wherein the or one said state determining operation is a shifting operation in which each designated one of the operating units sets said state of its own predicate register in dependence upon said state of the predicate register that precedes said own predicate register in said series.

14. A processor as claimed in claim 13, wherein each operating unit is designated in said shifting operation in the event that said control-information item corresponding to the unit's said own predicate register has said first value.

15. A processor as claimed in claim 10, wherein the or one said state determining operation is a shutting down operation in which each operating unit sets its said own predicate register to said second state in the event that the control-information item corresponding to that predicate register has said second value, and that said control-information item corresponding to the predicate register following said

own predicate register in said series has said first value.

16. A processor as claimed in claim 10, wherein the or one said state determining operation is a  
5 writing operation in which each designated one of the operating units sets its said own predicate register to a chosen one of said first and second states.

17. A processor as claimed in claim 16, wherein each operating unit has a data input for receiving a  
10 data signal indicating said chosen state.

18. A processor as claimed in claim 10, further comprising a completion detection unit which determines that a predetermined processor operation has been completed when, for every predicate register whose  
15 corresponding control-information item has said first value, the predicate register has said second state.

19. A processor as claimed in claim 18, wherein said completion detection unit comprise a plurality of individual completion detection circuits, each  
20 operating unit including one of said completion detection circuits of said plurality, and each said completion detection circuit is operable to produce a detection result for its particular operating unit based on said state of that unit's said own  
25 corresponding predicate register and on said control-information item corresponding to that predicate register.

20. A processor as claimed in claim 1, wherein each said operating unit includes combinatorial logic  
30 circuitry for effecting the or each said state determining operation.

21. A processor, operable to execute instructions on a predicated basis, comprising:

a series of predicate registers, each switchable  
35 between at least respective first and second states and each assignable to one or more predicated-execution

instructions;

a shifting register designating unit which designates one or more predicate registers of said series as respective shifting registers; and

5 a shifter connected with said predicate registers for carrying out a shift operation in which, for the or each predicate register designated by the shifting register designating means as such a shifting register, the state of the preceding register of said series is  
10 transferred into the register concerned, no such transfer being carried out into any register of said series not designated as such a shifting register.

22. A processor as claimed in claim 21, wherein said shifting register designating unit serves, when  
15 the processor is in use, to hold items of designation information corresponding respectively to said predicate registers of said series, each such item indicating whether or not the predicate register to which it corresponds is one of said shifting registers.

20 23. A processor as claimed in claim 22, wherein said designation-information items are changeable in use of the processor.